Scaling Effects on Thermal and Gate Induced Noise of Small Geometry LDD Mosfets

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Abstract

An analytical model is developed to study the impact of scaling on the thermal and gate induced noise of the small geometry LDD MOSFETs. The analyses includes the short channel, narrow width, velocity saturation, hot carrier and LDD effects. The intricacy in analysis when considering all these effects simultaneously as in the small geometry devices is overcomed and a generalized expression valid in the submicrometer range of device operation is developed. The results so obtained for effective current noise gain are compared with the measured results of short channel LDD MOSFETs and are found to be in good agreement. The results show that at frequencies much below the cut-off frequency, the drain noise is just 1% or even less of the gate induced noise. A comparison of the effective current noise gain in conventional and LDD MOSFETs is also done for the first time and it is observed that the current noise gain is higher in conventional MOSFETs than in the LDD MOSFETs because of the n^- series resistance. It is also observed that while the thermal noise increases with the decrease in device length, the gate induced noise decreases with the decrease in device length. A reversal of trends is observed when the device width is scaled down.

Key Words : LDD MOSFET, THERMAL NOISE, INDUCED GATE NOISE, CURRENT GAIN

Introduction

The progress in microprocessor and communication industry is hinged to the downscaling of the MOSFETs used in these devices. However, the downscaling of MOS devices have resulted in high unity gain frequencies of tens of GHz. At such high frequencies, the device reliability is at stake because of the noise inherent in the device itself. Therefore, an accurate analysis of the noise mechanisms operating in the submicron regime of device operation is essential. While the impact of scaling the device length on the thermal noise of conventional [1-3] and LDD MOSFETs [4] has been studied earlier but no model has been developed to analyze the effect of scaling the device area in these devices. Some simulated results are also available for the gate induced noise and current gain of short channel LDD MOSFETs [5] but the impact of scaling the device area on this noise too has not been analyzed so far. This is because when the device area is scaled down, the short channel, narrow width, the LDD, the velocity saturation effect and the DIBL effect have to be considered and this leads to a complexity in analysis. The present model overcomes this intricacy in analysis to develop an expression for the thermal and gate induced noise of the small geometry LDD MOSFETs.

Model Formulation

The drain current in strong inversion for an *n*-channel *LDD MOSFET* is given by [6]

$$I_{ds} = -\mu W Q_m \frac{dV_m}{dy} \quad (1)$$

where W is the effective channel width, μ represents the effective field dependent mobility given by [7] and Q_m is the electron density per unit area along the channel

$$Q_m = qN = Q_e - C_{ox}(V_{mg} - V_m) \quad (2)$$

where N is the number of channel carriers per unit area and $V_m (=V+\phi_B)$ is the channel potential with respect to the neutral substrate. V is the channel voltage at any point between source and drain and $\phi_B = \phi_{fn} + \phi_{fp}$ is the p-n junction barrier height [6]. V takes the values V_G, V_S and V_D, while V_m takes the values V_{mg}, V_{ms} and V_{md} at the gate, source and drain terminals respectively [7]. C_{ox} is the gate oxide capacitance per unit area, Q_e represents the extra charge due to the small geometry effects (which includes both the short channel and narrow width effects simultaneously) and the drain induced barrier lowering (*DIBL*) (which is rather suppressed in the *LDD* devices due to the voltage drop in the n^- region) is given by

$$Q_e = C_{ox}\left(\sqrt{\phi_S - V_{BS}}\left(K_1 - K_2\sqrt{\phi_S - V_{BS}}\right) - \Delta V_{TH} + K_w\sqrt{\phi_S - V_{BS}}\right) \quad (3)$$

where

ϕ_S represents the surface potential [6] and V_{BS} is the back bias. K_1 and K_2 are the two body factors, accounting for the non-uniformity of the short channel behavior and channel implantation effect. The expressions for K_1 and K_2 in terms of channel length L are developed using Lagrangian interpolation technique from the variation of $K_L \left(= K_1 - K_2\sqrt{\phi_S - V_{BS}}\right)$ and $\sqrt{\phi_S - V_{BS}}$ [6] and are given as

$$K_1 = 0.013(L)^3 10^{-18} - 0.227(L)^2 10^{-12} + 0.952(L)10^{-6} - 0.238 \quad (4)$$

$$K_2 = 3.686(L)^3 10^{-14} - 2.488(L)^2 10^{-9} - 0.0346(L) 10^{-6} + 0.276 \quad (5)$$

The expressions for K_w which represents the effective narrow gate body factor is given by [7]. The threshold voltage reduction due to *LDD* region (including the *DIBL* factor) represented as ΔV_{TH} is also given by [7]

Integrating (1) using (2) between the source and the drain an expression for drain current in the linear region can be obtained as

$$I_{ds} = -\mu\frac{W}{L}\left(\frac{C_{ox}}{2}(V_{md}^2 - V_{ms}^2) - C_{ox}V_{mg}(V_{md} - V_{ms})\right) - \mu\frac{W}{L}Q_e(V_{md} - V_{ms}) \quad (6)$$

Thermal Noise

Thermal noise is the most important source of noise in semiconductor devices in the microwave region. The thermal noise within the channel gives rise to both drain channel noise and induced gate noise. From [3], the expression for thermal (drain channel) noise is given by

$$S_{Id} = \frac{4kT}{L^2 I_{ds}} \int_{V_{ms}}^{V_{md}} (\mu W Q_m)^n S_0 \quad (7)$$

where

$$S_0 = \left(\mu W Q_m - \frac{I_{ds}}{E_c}\right)^{2-n} dV \quad (8)$$

with $0 \leq n \leq 2$

Taking n=2 and using (2) and (6) we get

$$S_{Id} = \frac{4kT}{L^2 I_{ds}} \left(\mu^2 W^2 \left(\frac{C_{ox}^2}{3} SI_{d1}\right) + S_2 + S_3\right) \quad (9)$$

where

$$SI_{d1} = (V_{md}^3 - V_{ms}^3) + (V_{ms}^2 - V_{ms}^2)(Q_e C_{ox} - C_{ox}^2 V_{mg}) + (V_{md} - V_{ms}) S_1) \quad (10)$$

where

$$S_1 = (Q_e^2 - 2 C_{ox} Q_e V_{mg} + C_{ox}^2 V_{mg}^2) \quad (11)$$

Gate Induced Noise

This noise is the diffusion noise generated by the carriers in the channel region, which are capacitatively coupled to the gate port. From [3], the expression for induced gate noise is given as

$$S_{Ig} = \frac{4kTC_{ox}^2 W^2 \omega^2}{I_{ds}^3} \int_{V_{ms}}^{V_{md}} (\mu W Q_m)^n S g_1 \quad (12)$$

where

$$Sg_1 = \left(\mu W Q_m - \frac{I_{ds}}{E_c}\right)^{2-n} (V_{as} - V)^2 dV \quad (13)$$

Taking n=2, we get

$$S_{Ig} = \frac{4kTC_{ox}^2 W^2 \omega^2}{I_{ds}^3} (S_{Ig1} + S_{Ig2} + S_{Ig3} + S_{Ig4} + S_{Ig5}) \quad (14)$$

$$S_{Ig1} = \frac{C_{ox}^2}{5} (V_{md}^5 - V_{ms}^5) \quad (15)$$

$$S_{Ig2} = \frac{C_{ox} (V_{md}^4 - V_{ms}^4) (Q_e - C_{ox} (V_{as} + V_{mg}))}{2} \quad (16)$$

$$S_{Ig3} = \frac{(V_{md}^3 - V_{ms}^3)(-2Q_e C_{ox}(2 V_{as} + V_{mg}) + S_{Ig31})}{3} \quad (17)$$

$$S_{Ig31} = (Q_e^2 + C_{ox}^2 (V_{as}^2 + V_{mg}^2 + 4V_{as} V_{mg})) \quad (18)$$

$$S_{Ig4} = ((-C_{ox}^2 V_{as} V_{mg} (V_{as} + V_{mg}) + S_{Ig41}) (V_{md}^2 - V_{ms}^2), \quad (19)$$

$S_{lg41} = (V_{as} Q_e (2 C_{ox} V_{mg} - Q_e + V_{as} C_{ox}))$
(20)

$S_{lg5} = V_{as}^2 (Q_e - C_{ox} V_{mg})^2 (V_{md} - V_{ms})$ (21)

Results and Discussion

Fig.2 depicts the variation of drain current with drain voltage for different gate voltages when the length and width are scaled simultaneously to the submicrometer range. The close agreement of the modelled and experimental result [8] in the linear region as well as when the device is driven into saturation establishes the validity of the model. The expression for drain current in the saturation region is given by [7]

Fig.3 shows the variation of the thermal noise with length at different gate voltages. It is clear that the thermal noise increases drastically with the decrease in length and with the increase in the device width. This is attributed to the increased hot-electron effect at small device lengths. The increasing electric field causes more carriers to reach velocity saturation thus increasing the amount of diffusion noise near the drain. However, when we decrease the channel width, although the lateral electric field increases but the number of mobile carriers in the channel decreases due to their neutralization by the opposite charge entering the channel from the substrate. Thus the amount of diffusion noise decreases when we scale the channel width.

Fig. 4 shows the ratio (S_{Id}/ S_{Ig}) which represents the effective current noise gain seen from the gate port to the drain port. It is seen that at frequencies much lower than the cut-off, the contribution of gate noise at the output is a very small fraction of the drain current noise. However, this fraction increases at higher frequencies because the carriers acquire enough energy to surmount the Si-SiO_2 barrier and

capacitatively couple onto the gate node as a gate current. A comparison of the effective current noise gain in conventional and LDD devices shows that current noise gain is higher in conventional MOSFETs than in LDD MOSFETs because of the clouding of electrons under the spacer in LDD devices which account for the increased drain channel noise.

Fig.5 Shows the variation of gate induced noise with the device dimensions. Noise increases with the decrease in device width while it decreases with the decrease in channel length. This is because at short channel lengths, the drain becomes the second gate and dominates the flow of electrons thereby causing them to saturate before they can be coupled to the gate port. However, when the channel width is scaled, the lateral electric field dominates and a quite a number of carriers get capacitatively coupled to the gate port, thereby increasing the gate noise.

Conclusion

An analytical model has been presented to characterize thermal and gate induced noise in the small geometry *LDD MOSFETs*. An accurate analysis of channel charge is done for the first time considering the short channel, narrow

width and *LDD* effects. It is observed that at low frequencies, the gate-induced noise is only 1% or even less of the drain noise and the fraction increases as we approach the cut-off frequency. Scaling trends show that thermal noise increases with the decrease in channel length and decreases with the decrease in channel width while the induced gate noise shows a reverse behavior. Thus a correct optimization of device dimensions is required to minimize the high frequency noise in LDD MOSFETs. Since the thermal noise is the key reliability issue at frequencies much lower than the cut-off frequency of the device, while the gate induced noise becomes important at relatively higher frequencies, the optimization of device dimensions depends on the operating frequency.

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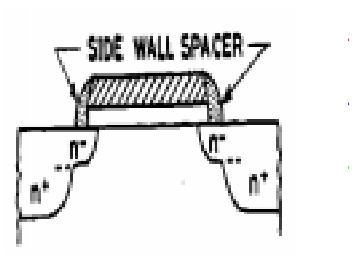

Fig1. Cross-section of an LDD MOSFET

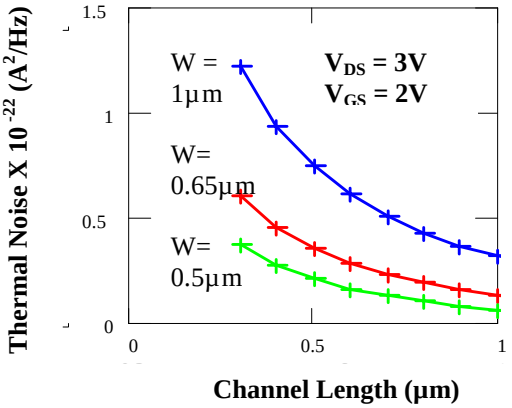

Fig.3 Variation of Thermal Noise with Length for small geometry LDD MOSFETs at different device widths.

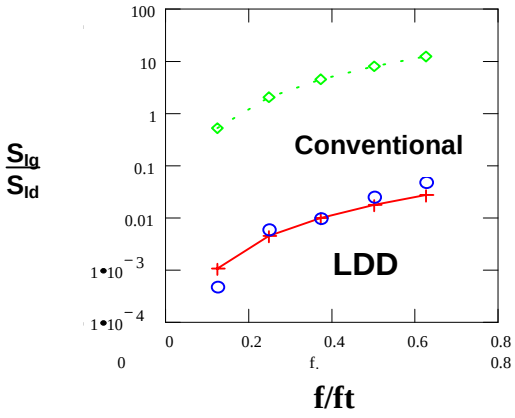

Fig.4 Variation of S_{lg}/ S_{ld} with f/ft + - + - + (Model), 0 0 0 (Experimental) at L= 0.5 µm, V_{DS} = 3V, V_{GS} = 2V

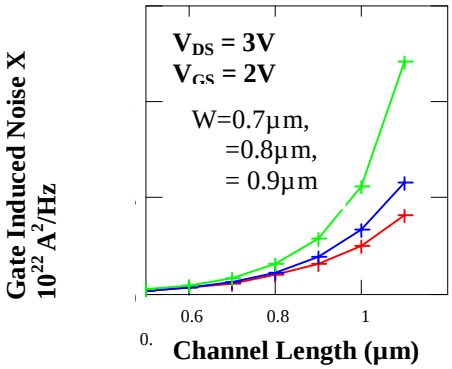

Fig.5 Variation of Induced Gate Noise with Length for small geometry LDD MOSFETs at different device widths.

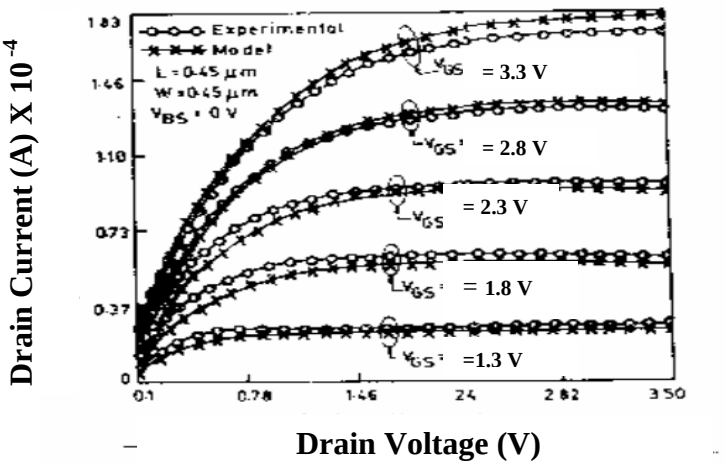

Fig.2 Variation of drain current with drain voltage at different gate bias